One particular advantage of the disclosed invention is that it can be very easily implemented (in at least some processes) by a simple transposition of steps (depositing the low-temperature oxide before, rather than after, the second layer of spin-on glass).

FIG. **4** shows a sample device structure incorporating a planarization layer according to the disclosed innovations. In this example, the partially fabricated device structure included active devices **12** in a substrate **10**, including polysilicon lines **14**. Field oxide **13** provides lateral separation active devices. Metal lines **18** overlie a first interlevel dielectric **16** (e.g. of BPSG over TEOS), and make contact to active device areas at contact locations **20**. (This provides the starting structure on which planarization is performed as described above.) A planarization layer **22** is then deposited, by the techniques described above, to reduce or eliminate the topographical excursions of the structure. An interlevel dielectric **24** overlies the planarization layer **22** (and the rest of the planarized structure), and includes via holes **25** through which a second metal layer **26** contacts the first metal layer **18**. The structure shown can be topped by a protective overcoat (not shown) through which holes are etched to expose locations of contact pads in the second metal layer.

Further Modifications and Variations

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

The disclosed innovative steps have been described in the context of via formation (e.g. forming connections from second metal to first metal, or third metal to second metal). Due to the accumulated topographical excursions, planarization is especially desirable at these stages. However, the disclosed innovative concepts can also be applied to planarization of lower levels as well.

The disclosed innovative concepts can also be applied to other spin-on materials, such as polyimide or polymethylmethacrylate.

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given.

What is claimed is:

1. An integrated circuit fabrication method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure which has an uneven topography containing high points;

(b.) applying and curing spin-on glass, to form a first dielectric;

(c.) depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer;

(d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;

(e.) performing a global etchback to substantially remove said dielectric stack from said high points of said partially fabricated structure;

(f.) deposition of an interlevel dielectric;

(g.) etching holes in said interlevel dielectric in locations; and

(h.) depositing and patterning a metallization layer to form a pattern of connections, including connections through said holes.

2. The method of claim **1**, wherein said deposition step (c.) is plasma-enhanced.

3. The method of claim **1**, wherein said deposition step (c.) uses TEOS as a source gas.

4. The method of claim **1**, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

5. The method of claim **1**, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

6. The method of claim **1**, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

7. The method of claim **1**, wherein said interlevel dielectric is a doped silicate glass.

8. An integrated circuit fabrication method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure which has an uneven topography containing high points;

(b.) applying and curing spin-on glass, to form a first dielectric;

(c.) depositing silicon dioxide under vacuum conditions, to form a second dielectric layer over said first layer;

(d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;

(e.) performing a global etchback to substantially remove said dielectric stack from said high points of said partially fabricated structure;

(f.) deposition of an interlevel dielectric;

(g.) etching holes in said interlevel dielectric in locations; and

(h.) depositing and patterning a metallization layer to form a pattern of connections, including connections through said holes.

9. The method of claim **8**, wherein said deposition step (c.) is plasma-enhanced.

10. The method of claim **8**, wherein said deposition step (c.) uses TEOS as a source gas.

11. The method of claim **8**, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

12. The method of claim **8**, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

13. The method of claim **8**, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

14. The method of claim **8**, wherein said interlevel dielectric is a doped silicate glass.

15. An integrated circuit fabrication method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure which has an uneven topography containing high points;